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10/685,508	10/16/2003	Kyu-Sung Kim	1349.1248	5074

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EXAMINER	
NGUYEN, LAM S	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,508	KIM, KYU-SUNG	
	Examiner	Art Unit	
	LAM S. NGUYEN	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Becerra et al. (US 5917509).

Becerra et al. discloses a device for transmitting serial data/addresses for a printer head in an interface unit transmitting firing information to the printer head with plural firing nozzles, comprising:

a data processing unit which provides:

input data comprising simultaneous firing nozzle data and data for determining a nozzle group firing direction (*FIG. 7, element DATA/DIRECTION*), and

a fire pulse (*FIG. 7, element ENABLE*);

a firing group direction data line (*Fig. 7: DATA/DIRECTION LINE 71*) which provides the input data to the printer head;

a fire pulse line which provides the fire pulse to the printer head (*Fig. 7: The ENABLE line 73*);

a selection unit which selects simultaneous firing nozzles based on the simultaneous firing nozzle data and the fire pulse (*FIG. 7, elements 82, 88, 80, and 78*);

a bi-directional shift register (*FIG. 7, element 90*) which generates firing nozzle

group selection signals; and

a unit which fires the selected nozzles based on the firing nozzle group selection signals (*FIG. 7, elements 74*).

Referring to claim 5: wherein the selection unit further comprises first memories (*FIG. 7, elements 82, 88*) which store the simultaneous firing nozzle data (*FIG. 7, element 82*) and the nozzle group firing direction data (*FIG. 7, element 88*), the first memories having one more in number than a number of the simultaneous firing nozzles (*FIG. 7: The number of the simultaneous firing nozzles is the same the number of registers in element 82*).

Referring to claim 6: further comprises second memories (*FIG. 7, element 80*) which store the simultaneous firing nozzle data, the second memories having a same number as a number of the simultaneous firing nozzles.

Referring to claim 7: wherein the selection unit further comprises a first plurality of logic AND gates (*FIG. 7, element 78*), each of which logic-ANDs a portion of the simultaneous firing nozzle data and the fire pulse signal, a number of the logic and gates being the same as a number of the simultaneous firing nozzles.

Referring to claim 8: wherein the selection unit further comprises: a second plurality of logic AND gates, each of which logic ANDs an output of one of the plurality of first logic AND gates and one of the nozzle group selection signals of the bi-directional shift register, a number of the second plurality of logic AND gates being the same as a number of the nozzles of the printer head (*FIG. 7, elements 74*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becerra et al. (US 5917509) in view of Edelen et al. (US 6547356).

Becerra et al. discloses the claimed invention as discussed above except and also teaches first memories for storing the firing group data and direction data (*FIG. 7, elements 82, 88*), second memories for storing outputs of the first memories in synchorization with a latch clock (*FIG. 7, element 80*), AND gates (*FIG. 7, element 78*) for ANDing respective outputs of the second memories and the fire pulse signal to generate nozzle firing signals (**Referring to claim 2**), and other AND gates for ANDing the nozzle firing signals and the outputs of the nozzle group selection signals of the bi-directional shift register (*FIG. 7, element 74*) (**Referring to claim 3**).

However, Becerra et al. does not disclose wherein the firing group data and the direction data are stored in the first memories in synchronization with a shift clock (**Referring to claim 2**).

Edelen et al. discloses a print data loading circuit for receiving N bits print data (*FIG. 1: Bits corresponding to R1-RN-1*) and an extra bit (*FIG. 1: Bit corresponding to RN*), wherein the both data are stored in the circuit in synchronization to a shift clock (*FIG. 1, signal CL1*).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the configuration of the selection unit disclosed by Becerra et al. so both, the firing group data and the direction data, are synchronized to the same shift clock as

disclosed by Edelen et al. since this has been held a well known technique in the art to ensure that the direction data bit is ready only when all data bits are shifted into the memory.

3. Claims 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becerra et al. (US 5917509) in view of Edelen et al. (US 6547356) and Moriat et al. (US 6511160).

Referring to claims 9, 14:

Becerra et al. discloses a device for generating signals for simultaneously firing nozzles of a printer head, the printer head comprising X groups of nozzles (*FIG. 7: Number groups of nozzles equal to number of banks, so X = 32*) with Y nozzles in a group (*FIG. 7: Each bank has four printing elements 46, so Y = 4*), where X and Y are integers, the device comprising:

a data processing unit which provides:

serial input data comprising Y bits which define specific nozzles of a group to be fired simultaneously and an additional bit (*FIG. 7: The DATA/DIRECTION input; The additional bit is the direction bit*),

a shift clock (*FIG. 7: The BIT SHIFT input*),

a latch clock (*FIG. 7: The LCLK*), and

a fire pulse (*FIG. 7: The ENABLE input*);

a converter (*FIG. 7, elements 82, 88*) which outputs the Y bits as parallel data in response to the shift clock;

a Y bit latch (*FIG. 7, element 80*) which latches the parallel Y bits in response to the latch clock;

a first logic AND unit (*FIG. 7, element 78*) which logic ANDS each of the parallel Y bits and the fire pulse, to output Y nozzle selection signals;

a bi-directional shift register (*FIG. 7, element 90*) having a shift direction input (*FIG. 7, element DIR*), X+2 parallel outputs comprising an MSB, an LSB (*FIG. 7, element 90: Two END REGISTERS*) and X outputs between the MSB and the LSB, wherein values of the X parallel outputs are shifted in response to a SCLK clock and the additional bit;

a second logic AND unit (*FIG. 7, element 74*) which logic ANDS each of the X outputs with each of the Y nozzle selection signals to output the simultaneous firing nozzle signals.

- Becerra et al. does not disclose wherein the converter outputs the additional bit as parallel to the Y bits in response to a shift clock.

Edelen et al. discloses a print data loading circuit for receiving N bits print data (*FIG. 1: Bits corresponding to R1-RN-1*) and an additional bit (*FIG. 1: Bit corresponding to RN*), wherein the circuit outputs the N bits and the additional bit as parallel data in response to a shift clock (*FIG. 1, signal CL1*).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the configuration of the selection unit disclosed by Becerra et al. so both, the firing group data and the direction data, are synchronized to the same shift clock as disclosed by Edelen et al. to ensure that the direction data bit is ready only when all data bits are shifted into the memory as a well known technique in the art.

- In addition, Becerra et al. does not also disclose wherein the Y bit latch and the bi-directional shift register operate in response to the same latch clock.

Morita et al. discloses an ink jet printhead having a driving circuit including a 4-bit latch (*FIG. 1, element 22*) and a bidirectional shift register (*FIG. 13, element 24*), wherein the 4-bit

latch and the bi-directional shift register operate in response to the same latch clock (*FIG. 13: Signal ENABLE*).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the configuration disclosed by Becerra et al. so both the latch and the bi-directional shift register are operated to the same latch clock as disclosed by Morita et al. since this is a common technique well known in the art to ensure the synchronism between the outputs of the latch and the outputs of the bi-directional register.

Becerra et al. also discloses the following claimed invention:

Referring to claims 10-11, 15: wherein the MSB and the LSB of the bi-directional shift are each initially preloaded with data of "1" prior to the values of the X parallel outputs being shifted (*column 12, lines 12-15: The two end cell 98 supply the initial tokens for both the main token and the prepulse token inputs*) and wherein values of the X parallel outputs are shifted in a first direction where the additional bit has a value of 1 and are shifted in a second direction where the additional bit has a value of 0 (*column 11, lines 47-51*).

Referring to claim 12: wherein the first logic AND unit comprises Y AND gates (*FIG. 7, element 78: Number of AND gates equals to number of data bits*).

Referring to claim 13: wherein the second logic unit comprises X*Y AND gates (*FIG. 7, elements 74: Number of AND gates (74) = 4 (number of data bits) * 32 (number of groups)*).

Response to Arguments

Applicant's arguments filed 11/22/2005 have been fully considered but they are not persuasive.

The applicant argued that Becerra does not disclose determining data for determining simultaneous firing nozzles. In response, the examiner cites that Becerra's DATA/DIRECTION LINE (71) conveys two kinds data bits: DATA bits and DIRECTION bits. The DATA bits are latched into the serial latch (82) and then the parallel latch (80). Next, the DATA bits are encoded by the logical AND gates (78) and the OR gates (76), and passed out to the data lines (94) (*column 7, lines 10-42*), wherein the signals on each data line are provided to a particular group of resistance heaters to cause ink ejection through associated nozzles. For example, a signal on a data line (94) connected to the output of the top OR gate (76) drives a group of all leftmost heaters in every banks (96) through associate predrivers (74). Similarly, a signal on a data line (94) connected to the output of the bottom OR gate (76) drives a group of all rightmost heaters in every banks (96) through associate predrivers (74). As a result, Becerra's DATA bits reads on the data for determining simultaneous firing nozzles as claimed since they represent a signal that can drive (or determine) all heaters (or nozzles) in a certain group (all leftmost heaters or all rightmost heaters, for example) at the same time.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S. NGUYEN whose telephone number is (571)272-2151. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEPHEN D. MEIER can be reached on (571)272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
01/10/2006

Hai Pham

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PRIMARY EXAMINER